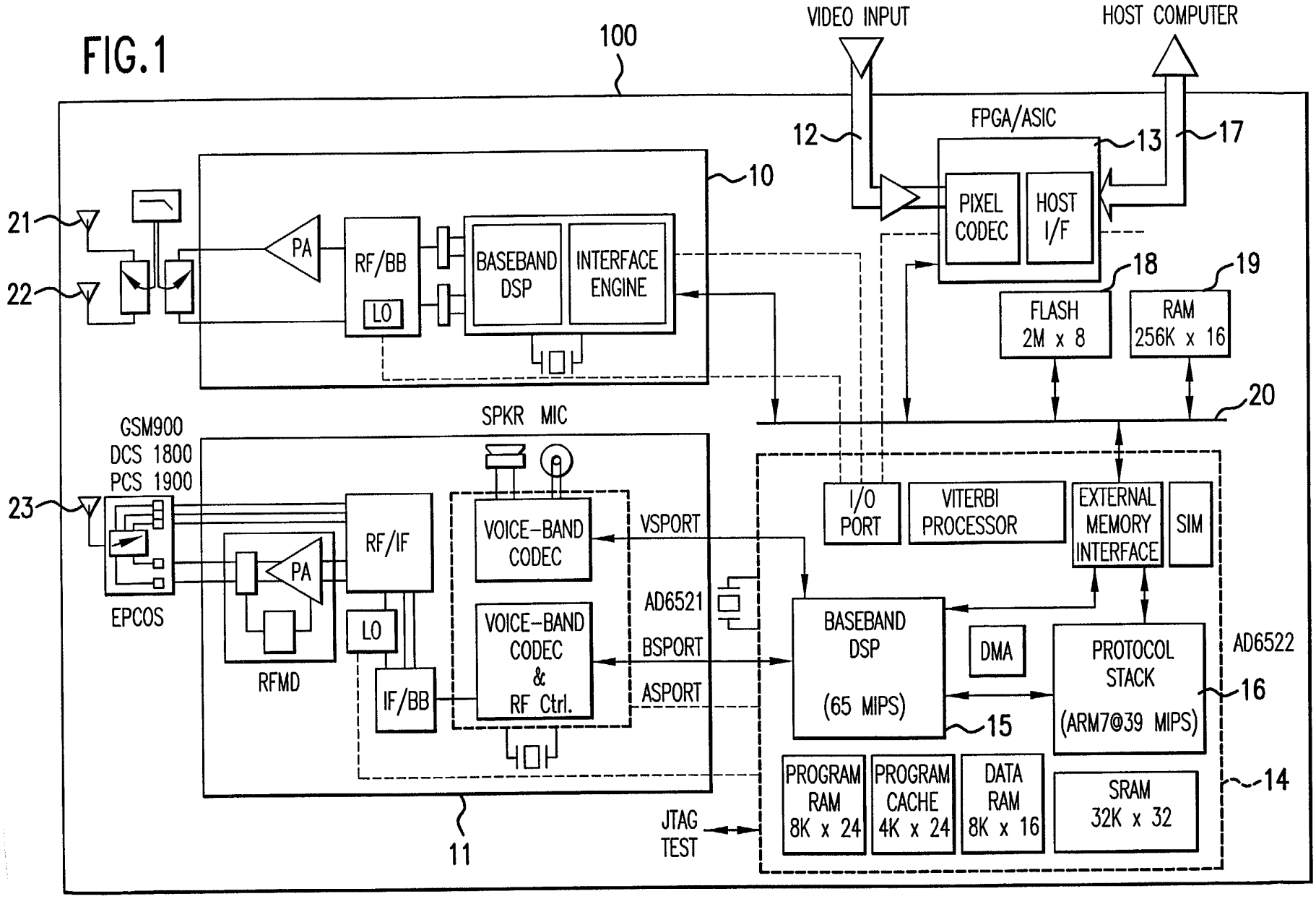
FIG.1


100
VIDEO INPUT
HOST COMPUTER
FPGA/ASIC
12
13
17
10
21
22
PA
RF/BB
LO
BASEBAND DSP
INTERFACE ENGINE
PIXEL CODEC
HOST I/F
18
19
FLASH 2M x 8
RAM 256K x 16
20
SPKR MIC
GSM900
DCS 1800
PCS 1900
23
EPCOS
RFMD
RF/IF
VOICE-BAND CODEC
VSPORT
AD6521
VOICE-BAND CODEC & RF Ctrl.
BSPORT
ASPORT
IF/BB
11
I/O PORT
VITERBI PROCESSOR
EXTERNAL MEMORY INTERFACE
SIM
BASEBAND DSP
(65 MIPS)
DMA
PROTOCOL STACK
(ARM7@39 MIPS)
AD6522
16
15
PROGRAM RAM 8K x 24
PROGRAM CACHE 4K x 24
DATA RAM 8K x 16
SRAM 32K x 32
14
JTAG TEST